PATENT ABSTRACTS OF JAPAN

(11)Publication number : 10-020052

(43)Date of publication of application : 23.01.1998

(51)Int.Cl. G04G 3/02
G01R 23/10

(21)Application number : 08-171275

(22)Date of filing : 01.07.1996

(71)Applicant : YAZAKI CORP

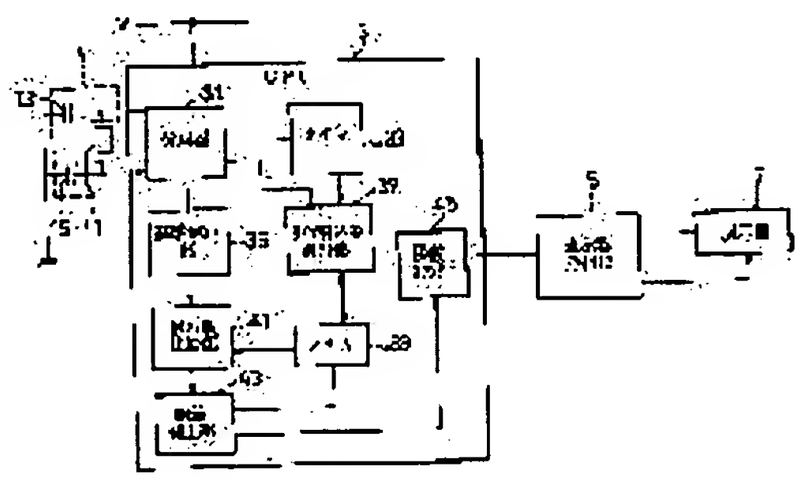
(72)Inventor : NAGAOKA KYOICHI

(54) TIME CORRECTION METHOD AND DEVICE THEREFOR

(57)Abstract:

PROBLEM TO BE SOLVED: To provide a time correction device correcting a time error generated when basic oscillation frequency generated in a basic oscillator is divided by means of a frequency divider.

SOLUTION: A reference count unit 35 divides a unit time by a clock cycle of a signal outputted from a frequency divider 31 to a timer 33 so as to find a reference count number. A timer interruption count unit 37 divides a timer 33 interrupting time set in the timer 33 by the clock cycle so as to find an interruption count number and sequently adds the interruption count number every time when timer 33 interruption is generated. An error correcting unit 43 subtracts the reference count number from the addition interruption count number if the provided addition interruption count number exceeds the reference count number, and the excessive count number is used as an initial value of the addition interruption count number in generation of the following timer 33 interruption, and consequently, a time error can be corrected.



LEGAL STATUS

[Date of request for examination]

[Date of sending the examiner's decision of

[JP,10-020052,A]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the time-of-day error assistant square method which amends the time-of-day error generated when dividing of the basic oscillation frequency oscillated with the basic oscillator used for information processors, such as a microcomputer, is carried out with a counting-down circuit, and its equipment.
[0002]
[Description of the Prior Art] In information processors, such as a microcomputer, dividing of the basic oscillation frequency oscillated with the crystal oscillator is carried out with a counting-down circuit, and timing of each part in a microcomputer is planned using this clock signal by which dividing was carried out. For example, the clock signal by which dividing was carried out is supplied to a timer counter, and counting of the time of day is carried out by timer interruption.
[0003] this kind of the former [drawing 4] of time of day -- counting -- an approach is shown. First, the clock period of said signal by which dividing was carried out is determined, and it decides on the timer interruption time amount by the timer counter further (step S101).
[0004] Next, when it is judged whether timer interruption occurs (step S103) and timer interruption occurs, a timer counter adds 1 to counted value (step S105).
[0005] And the timer counter carries out counting of the number of clocks of the clock signal which has clock period a in 1 second and by which dividing was carried out, as shown in drawing 5 . Furthermore, it is judged whether 1 second passed (step S107).
[0006] A timer counter is cleared when 1 second passes (step S109). Furthermore, as for the number counter of seconds, only 1 increments counted value (step S111).
[0007] And it is judged for the counted value of the number counter of seconds whether it is 60 (for 1 minute) (step S113), and when the counted value of the number counter of seconds is not 60, it returns to processing of step S103.
[0008] Furthermore, when the counted value of the number counter of seconds is set to 60, it is judged for other processings, for example, processing of the count of a fraction counter etc., whether it is termination (step S115).
[0009]
[Problem(s) to be Solved by the Invention] However, dividing of the basic oscillation frequency oscillated with the crystal oscillator may be carried out with a counting-down circuit, and a time-of-day error may occur in this clock signal by which dividing was carried out.
[0010] For example, it means that the timer counter had counted clock period [of n pieces] a at the time of 1-second progress as shown in drawing 5 . That is, n time amount of clock period a is larger than 1 second, and the part shown in a shadow area serves as a time-of-day error.
[0011] Since this time-of-day error is not amended, if the timer counter counts clock period [of n pieces] a 2 seconds or more, said time-of-day error is accumulated with

time amount. For this reason, there was a problem that the precision of a clock fell.
[0012] The purpose of this invention amends the time-of-day error, when a time-of-day error is in the dividing signal which carried out dividing of the reference clock signal, and it offers the time-of-day error assistant square method which can improve the precision of a clock, and its equipment.
[0013]
[Means for Solving the Problem] The following means were used for this invention in order to solve said technical problem. In the time correction equipment which amends the time-of-day error generated when invention of claim 1 carries out dividing of the basic oscillation frequency oscillated with the basic oscillator with a counting-down circuit The criteria count area which asks for the criteria number of counts by doing the division of the unit time amount with the clock period of the signal outputted to a timer from a counting-down circuit, The timer interruption count area which asks for the interruption number of counts and carries out sequential addition of the interruption number of counts for every timer interruption generating by doing the division of the timer interruption time amount set as the timer with said clock period, The obtained addition interruption number of counts the criteria number of counts When you exceed, let it be a summary to have the error assistant positive part which amends a time-of-day error by subtracting the criteria number of counts from the addition interruption number of counts, and making the remainder number of counts into the initial value of the addition interruption number of counts at the time of next timer interruption generating.
[0014] When a criteria count area does the division of the unit time amount with the clock period of the signal outputted to a timer from a counting-down circuit, it asks for the criteria number of counts, and, according to this invention, a timer interruption count area carries out sequential addition of the interruption number of counts for every timer interruption generating in quest of the interruption number of counts by doing the division of the timer interruption time amount set as the timer with said clock period.
[0015] And an error assistant positive part amends a time-of-day error by subtracting the criteria number of counts from the addition interruption number of counts, and making the remainder number of counts into the initial value of the addition interruption number of counts at the time of next timer interruption generating, when the obtained addition interruption number of counts exceeds the criteria number of counts.
[0016] That is, since the time-of-day error of a dividing signal is amended by the error assistant positive part even if a time-of-day error occurs [the basic oscillation frequency oscillated with the basic oscillator] with a counting-down circuit, the precision of a clock can be improved.
[0017] Invention of claim 2 makes it a summary to repeat addition processing of the interruption number of counts by said timer interruption count area, and amendment processing of the time-of-day error by said error assistant positive part, and to perform them.
[0018] Since according to this invention addition processing of the interruption number of counts by the timer interruption count area and amendment processing of the time-of-day error by said error assistant positive part are repeated and are performed, the time-of-day error accumulated with the passage of time is amended.
[0019] In the time correction approach which amends the time-of-day error generated when invention of claim 3 carries out dividing of the basic oscillation frequency

oscillated with the basic oscillator with a counting-down circuit The 1st step which asks for the criteria number of counts by doing the division of the unit time amount with the clock period of the signal outputted to a timer from a counting-down circuit, The 2nd step which asks for the interruption number of counts by doing the division of the timer interruption time amount set as the timer with said clock period, The 3rd step which carries out sequential addition of the interruption number of counts for every timer interruption generating, The obtained addition interruption number of counts the criteria number of counts When you exceed, let it be a summary to include the 4th step which amends a time-of-day error by subtracting the criteria number of counts from the addition interruption number of counts, and making the remainder number of counts into the initial value of the addition interruption number of counts at the time of next timer interruption generating.

[0020] According to this invention, by doing the division of the unit time amount with the clock period of the signal outputted to a timer from a counting-down circuit, it asks for the criteria number of counts, and asks for the interruption number of counts at the 1st step by doing the division of the timer interruption time amount set as the timer at the 2nd step with said clock period.

[0021] A time-of-day error is amended by carrying out sequential addition of the interruption number of counts for every timer interruption generating, subtracting the criteria number of counts from the addition interruption number of counts, when the addition interruption number of counts obtained at the 4th step exceeds the criteria number of counts, and making the remainder number of counts into the initial value of the addition interruption number of counts at the time of next timer interruption generating at the 3rd step.

[0022] That is, even if a time-of-day error occurs [the basic oscillation frequency oscillated with the basic oscillator] with a counting-down circuit, since the time-of-day error of a dividing signal is amended, the precision of a clock can be improved.

[0023] Invention of claim 4 makes it a summary to repeat addition processing of said 3rd interruption number of counts of a step, and amendment processing of the time-of-day error of the 4th step, and to perform them.

[0024] Since according to this invention addition processing of the 3rd interruption number of counts of a step and amendment processing of the time-of-day error of the 4th step are repeated and are performed, the time-of-day error accumulated with the passage of time is amended.

[0025]

[Embodiment of the Invention] Hereafter, the time correction approach of this invention and its equipment are explained. The block diagram of the gestalt of operation of the time correction equipment of this invention is shown in drawing 1 .

[0026] The time correction equipment shown in drawing 1 is formed in information processors, such as a microcomputer, and amends the time-of-day error generated when dividing of the basic oscillation frequency oscillated with the basic oscillator is carried out with a counting-down circuit.

[0027] Time correction equipment consists of a central processing unit (CPU) 3 connected to the crystal oscillator 1 which is a basic oscillator, and a crystal oscillator 1, an indicator driver IC (integrated circuit) 5 connected to CPU3, and an indicator 7 connected to this.

[0028] A crystal oscillator 1 connects a capacitor 13 to one terminal, connects a capacitor 15 to an other-end child, and consists of a quartz resonator 11 which oscillates a basic clock signal with a basic oscillation frequency.
[0029] CPU3 has a counting-down circuit 31, a timer 33, the criteria count area 35, the timer interruption count area 37, memory 39, the number-of-counts comparator 41, the error assistant positive part 43, and the number counter 45 of seconds.
[0030] A counting-down circuit 31 carries out dividing of the basic clock signal with the basic oscillation frequency oscillated with the crystal oscillator 1, and outputs a dividing signal to a timer 33 and the criteria count area 35.
[0031] A timer 33 sets up timer interruption time amount, and when timer interruption time amount is reached, it generates timer interruption.
[0032] The criteria count area 35 asks for the criteria number of counts by inputting the dividing signal outputted from a counting-down circuit 31, and doing the division of the unit time amount with the clock period of a dividing signal.
[0033] The timer interruption count area 37 inputs the dividing signal from the timer interruption time amount and the counting-down circuit 31 from a timer 33, by doing the division of the timer interruption time amount with said clock period, asks for the interruption number of counts, and memorizes the interruption number of counts to the work area of memory 39.
[0034] Moreover, the timer interruption count area 37 adds the interruption number of counts memorized by memory 39 for every timer interruption generating to this interruption number of counts, is memorizing the addition interruption number of counts in memory 39, and carries out sequential addition of the addition interruption number of counts.
[0035] The number-of-counts comparator 41 compares the criteria number of counts from the criteria count area 35 with the addition interruption number of counts from memory 39.
[0036] The error assistant positive part 43 adds 1 to the counted value of the number counter 45 of seconds as what passed for 1 second, when the obtained addition interruption number of counts exceeds the criteria number of counts based on the output of the number-of-counts comparator 41.
[0037] When the obtained addition interruption number of counts exceeds the criteria number of counts, the error assistant positive part 43 subtracts the criteria number of counts from the addition interruption number of counts, and amends a time-of-day error with outputting the remainder number of counts to memory 39 as initial value of the addition interruption number of counts at the time of next timer interruption generating.
[0038] Moreover, addition processing of the interruption number of counts by said timer interruption count area 37, comparison processing of the number of counts of the number-of-counts comparator 41, and amendment processing of the time-of-day error by said error assistant positive part 43 are performed repeatedly two or more times.
[0039] The indicator driver IC 5 drives an indicator 7, and an indicator 7 displays the number information of seconds from the number counter 45 of seconds through the indicator driver IC 5.
[0040] Next, it explains with reference to the flow chart which shows the time correction approach of this invention constituted in this way, and actuation of the equipment to the block diagram of drawing 1 , and drawing 2 , and the timing chart shown in drawing 3 .

[0041] First, a counting-down circuit 31 carries out dividing of the basic clock signal with the basic oscillation frequency oscillated with the crystal oscillator 1, and outputs a dividing signal to a timer 33 and the criteria count area 35. In this case, the clock period of the dividing signal supplied to a timer 33 is determined from the division ratio of a basic oscillation frequency (step S11).
[0042] Next, it asks for the criteria number of counts by the criteria count area's 35 inputting the dividing signal outputted from a counting-down circuit 31, and doing the division of the 1 second (unit time amount) with said clock period of a dividing signal (step S13).
[0043] That is, if what clock is counted from the clock period of the dividing signal supplied to a timer 33, it will ask for whether it has been 1 second, and let the counted value be said criteria number of counts.
[0044] And the timer interruption count area 37 inputs the dividing signal from the timer interruption time amount and the counting-down circuit 31 from a timer 33, and it asks for the interruption number of counts by doing the division of the timer interruption time amount set up with the timer 33 with said clock period (step S15).
[0045] Next, it is judged whether the timer interruption by the timer 33 occurred (step S17).
[0046] When timer interruption occurs, the timer interruption count area 37 memorizes the interruption number of counts to the work area of memory 39 (step S19).
[0047] The number-of-counts comparator 41 compares the criteria number of counts from the criteria count area 35 with the interruption number of counts from memory 39 (step S21).
[0048] As shown in drawing 3 , since the interruption number of counts K2 is smaller than the criteria number of counts K1, it returns to processing of step S15. And the timer interruption count area 37 adds the interruption number of counts memorized by memory 39 to this interruption number of counts for every timer interruption generating, is memorizing the addition interruption number of counts in memory 39, and carries out sequential addition of the addition interruption number of counts.
[0049] And as shown in drawing 3 , the error assistant positive part 43 subtracts the criteria number of counts from the addition interruption number of counts, when the addition interruption number of counts (four sums of K2) from memory 39 exceeds the criteria number of counts K1.
[0050] Furthermore, the error assistant positive part 43 amends a time-of-day error (remainder number-of-counts **K21) by making memory 39 memorize remainder number-of-counts **K21 as initial value of the addition interruption number of counts at the time of next timer interruption generating (step S23).
[0051] That is, the addition interruption number of counts memorized by memory 39 is rewritten by remainder number-of-counts **K21.
[0052] Moreover, the error assistant positive part 43 adds 1 to the counted value of the number counter 45 of seconds as what passed for 1 second, when the obtained addition interruption number of counts exceeds the criteria number of counts (step S25).
[0053] Furthermore, when it is judged how [from which the counted value of the number counter 45 of seconds was set to 60] it is (step S27) and the counted value of the number counter 45 of seconds has not become 60, it returns to processing of step S17.
[0054] And processing of step S17 to the step S27 for the 2nd second is performed. In

this case, if timer interruption occurs, the timer interruption count area 37 adds remainder number-of-counts **K21 memorized by memory 39 to this interruption number of counts, is memorizing the addition interruption number of counts in memory 39, and carries out sequential addition of the addition interruption number of counts.
[0055] And as shown in drawing 3 , the error assistant positive part 43 subtracts the criteria number of counts from the addition interruption number of counts, when the addition interruption number of counts (four sums of K2) from memory 39 exceeds the criteria number of counts K1.
[0056] Furthermore, the error assistant positive part 43 amends a time-of-day error (remainder number-of-counts **K22) by making memory 39 memorize remainder number-of-counts **K22 as initial value of the addition interruption number of counts at the time of next timer interruption generating.
[0057] When a multiple-times repeat deed and the number counter 45 of seconds are set to 60 in amendment processing of such a time-of-day error, it is judged whether next processing is ended (step S29).
[0058] Thus, according to the time correction approach of this invention, and the gestalt of operation of the equipment, since the time-of-day error of a dividing signal is amended by the error assistant positive part 43 even if a time-of-day error occurs [the basic oscillation frequency oscillated with the crystal oscillator 1] with a counting-down circuit 31, the precision of a clock can be improved.
[0059] Moreover, since addition processing of the interruption number of counts by the timer interruption count area 37 and amendment processing of the time-of-day error by said error assistant positive part 43 are repeated and are performed, the time-of-day error accumulated with the passage of time is amended for every second, and the effectiveness is size.
[0060] In addition, this invention is not limited to the gestalt of said operation. With the gestalt of operation, in the flow chart shown in drawing 2 , after performing calculation processing of the criteria number of counts of step S13, calculation processing of the timer interruption number of counts of step S15 was performed.
[0061] For example, conversely, after performing calculation processing of the timer interruption number of counts, it may be made to perform calculation processing of the criteria number of counts with processing of the gestalt of operation.
[0062]
[Effect of the Invention] When a criteria count area does the division of the unit time amount with the clock period of the signal outputted to a timer from a counting-down circuit, it asks for the criteria number of counts, and, according to this invention, a timer interruption count area carries out sequential addition of the interruption number of counts for every timer interruption generating in quest of the interruption number of counts by doing the division of the timer interruption time amount set as the timer with said clock period.
[0063] An error assistant positive part amends a time-of-day error by subtracting the criteria number of counts from the addition interruption number of counts, and making the remainder number of counts into the initial value of the addition interruption number of counts at the time of next timer interruption generating, when the obtained addition interruption number of counts exceeds the criteria number of counts.
[0064] That is, since the time-of-day error of a dividing signal is amended by the error

assistant positive part even if a time-of-day error occurs [the basic oscillation frequency oscillated with the basic oscillator] with a counting-down circuit, the precision of a clock can be improved.

[0065] Moreover, since addition processing of the interruption number of counts by the timer interruption count area and amendment processing of the time-of-day error by said error assistant positive part are repeated and are performed, the time-of-day error accumulated with the passage of time is amended.

[0066] Furthermore, at the 1st step, by doing the division of the unit time amount with the clock period of the signal outputted to a timer from a counting-down circuit, it asks for the criteria number of counts, and asks for the interruption number of counts by doing the division of the timer interruption time amount set as the timer at the 2nd step with said clock period.

[0067] A time-of-day error is amended by carrying out sequential addition of the interruption number of counts for every timer interruption generating, subtracting the criteria number of counts from the addition interruption number of counts, when the addition interruption number of counts obtained at the 4th step exceeds the criteria number of counts, and making the remainder number of counts into the initial value of the addition interruption number of counts at the time of next timer interruption generating at the 3rd step.

[0068] That is, even if a time-of-day error occurs [the basic oscillation frequency oscillated with the basic oscillator] with a counting-down circuit, since the time-of-day error of a dividing signal is amended, the precision of a clock can be improved.

[0069] Moreover, since addition processing of the 3rd interruption number of counts of a step and amendment processing of the time-of-day error of the 4th step are repeated and are performed, the time-of-day error accumulated with the passage of time is amended.

CLAIMS

[Claim(s)]

[Claim 1] In the time correction equipment which amends the time-of-day error generated when dividing of the basic oscillation frequency oscillated with the basic oscillator is carried out with a counting-down circuit The criteria count area which asks for the criteria number of counts by doing the division of the unit time amount with the clock period of the signal outputted to a timer from a counting-down circuit, The timer interruption count area which asks for the interruption number of counts and carries out sequential addition of the interruption number of counts for every timer interruption generating by doing the division of the timer interruption time amount set as the timer with said clock period, The error assistant positive part which amends a time-of-day error by subtracting the criteria number of counts from the addition interruption number of counts, and making the remainder number of counts into the initial value of the addition interruption number of counts at the time of next timer interruption generating when the obtained addition interruption number of counts exceeds the criteria number of counts, Time correction equipment characterized by preparation ******.

[Claim 2] Time correction equipment according to claim 1 characterized by repeating addition processing of the interruption number of counts by said timer interruption count area, and amendment processing of the time-of-day error by said error assistant positive

part, and performing them.
[Claim 3] In the time correction approach which amends the time-of-day error generated when dividing of the basic oscillation frequency oscillated with the basic oscillator is carried out with a counting-down circuit The 1st step which asks for the criteria number of counts by doing the division of the unit time amount with the clock period of the signal outputted to a timer from a counting-down circuit, The 2nd step which asks for the interruption number of counts by doing the division of the timer interruption time amount set as the timer with said clock period, The 3rd step which carries out sequential addition of the interruption number of counts for every timer interruption generating, The 4th step which amends a time-of-day error by subtracting the criteria number of counts from the addition interruption number of counts, and making the remainder number of counts into the initial value of the addition interruption number of counts at the time of next timer interruption generating when the obtained addition interruption number of counts exceeds the criteria number of counts, ****** -- the time correction approach characterized by things.
[Claim 4] The time correction approach according to claim 3 characterized by repeating addition processing of said 3rd interruption number of counts of a step, and amendment processing of the time-of-day error of the 4th step, and performing them.

[Translation done.]